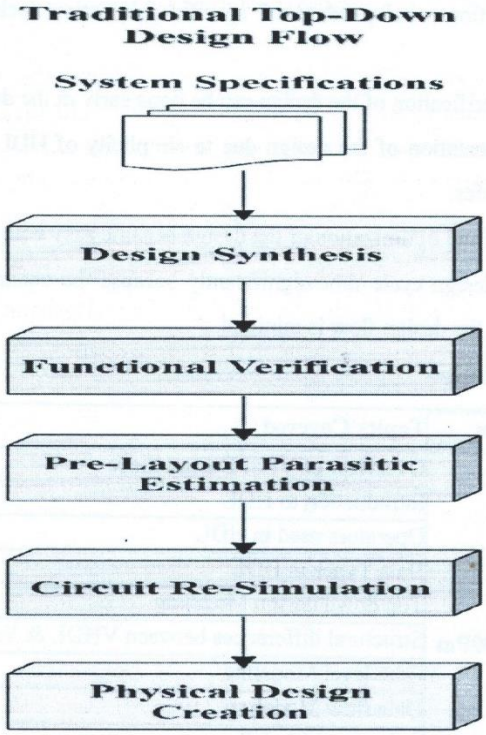
Report on VLSI Design Using Verilog HDL
Date: 17/02/2020

About VLSI Design

With the advent of VLSI technology and increased usage of digital circuits, designers have to design single chips with millions of transistors. It became almost impossible to verify these circuits of high complexity on breadboard. Hence Computer-aided techniques became critical for verification and design of VLSI digital circuits. As designs got larger and more complex, logic simulation assumed an important role in the design process. Designers could iron out functional bugs in the architecture before the chip was designed further. All these factors which led to the evolution of Computer-Aided Digital Design, intern led to the emergence of Hardware Description Languages.



Workshop on VLSI Design Using Verilog HDL:

This workshop is dedicated in training the students on the design and development of a VLSI circuits using the hardware description language Verilog HDL. This workshop is an invaluable resource for those who are learning VLSI design. Designing a hardware circuit using

HDL is not something that is completed in seconds. Design of digital integrated circuit requires a highly technical skill. The main objective of the workshop is to provide the basics of digital logic design using Verilog HDL as well as more advanced topics.

This is a one day program which focuses on the design and development of VLSI digital logic blocks using the Verilog HDL. Each participant will learn the key concepts for the design and develop digital logic circuits. Different types of circuit modeling such as gate level, data-flow and behavioral will be illustrated. Further, digital logic circuits simulation and verification is performed using advanced simulation tool.

Importance of HDLs

- RTL descriptions, independent of specific fabrication technology can be made an verified.
- Functional verification of the design can be done early in the design cycle.
- Better representation of the design due to simplicity of HDLs when compared to gate-level schematics.
- Modification and optimization of the design became easy with HDLs.
- Cuts down design cycle time significantly because the chance of a functional bug at a later stage in the design flow is minimal.

Workshop Schedule:

Day/Session	Topics Covered
10:00 AM- 1:00Pm	Overview of VLSI Design Flow
	Introduction to HDL
	Operators used in HDL
	Data Types in HDL
	Top down design Modeling
	Structural differences between VHDL & Verilog
	Gate level Modeling
	Data flow Modeling
	Behavioral Modeling
	Practical Modeling of the logics
1:30 PM- 4:30PM	**Practical:** Design & Synthesis of basic logic gates
	Practical: Design & Synthesis of up/down counters
	Practical: Design & Synthesis of Finite state Machine
	Practical: Design & Synthesis of UART
	Q&A

Workshop outcomes:

Hands on design, implement and functional verification of digital logic circuits using Verilog HDL. The workshop covers all the basics information related to VLSI design flow using Verilog. Performed different types of circuit modeling such as gate level, data-flow and behavioral and their simulations. This workshop is useful in the future while doing their academic projects or any scientific research in the college and industry.

Take Away by Participants:

- ✓ Learn & Interact with renowned Industry Experts.
- ✓ Receive an unparalleled education on the design and verification of digital VLSI with personal one-on-one attention.
- ✓ Covers all the basics of hardware description language Verilog HDL.
- ✓ Hands on experience of advanced technologies used for VLSI industry.
- ✓ Certificate of participation.

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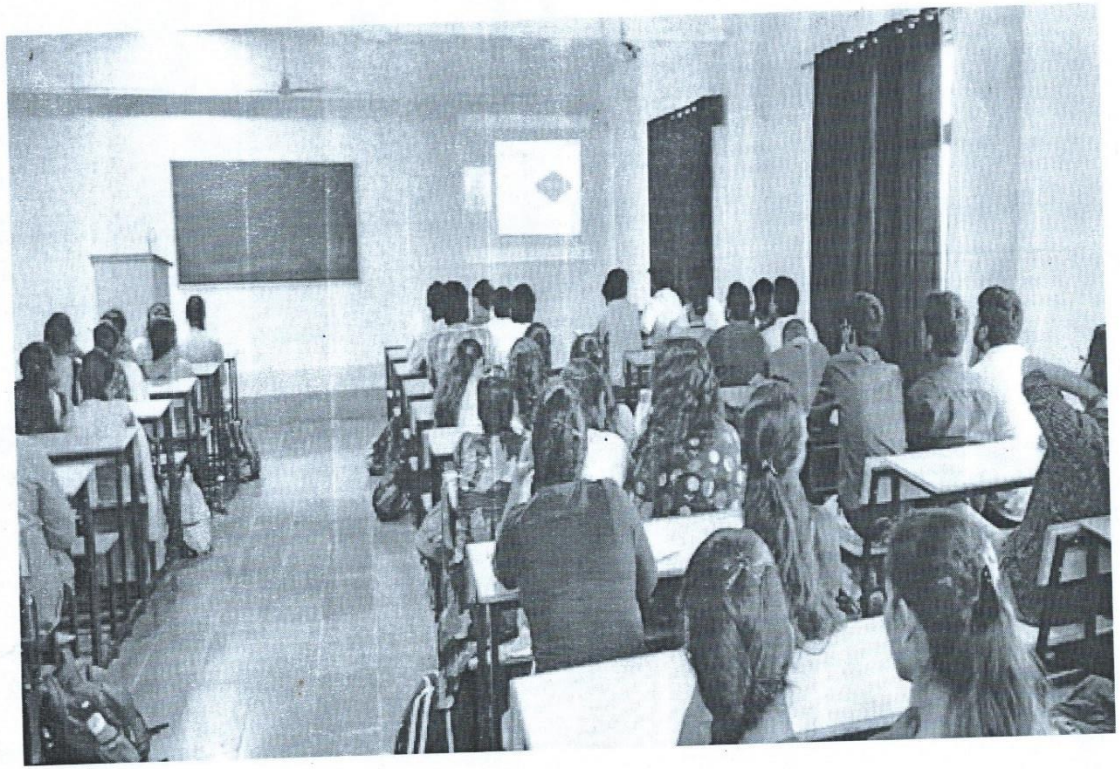

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