Nalla Narasimha Reddy Education Society's Group of Institutions
Integrated Campus - School of Engineering
(Autonomous)
Department of ECE

A Report on

One Week Workshop on Hands-On Training in VLSI Design

(17th October to 22nd October 2022)

Department of ECE successfully conducted one week workshop on hand-on training in VLSI Design for 4th B.Tech students on 17th October to 22nd October 2022. The aim of this workshop is to provide an overview on EDA tools for VLSI design to the participants. The workshop will comprise of live demonstration of tools and lectures delivered by Department faculty on platforms like Xilinx Vivado and Cadence Virtuoso.

The participants will have exposure to the state-of-the-art semiconductor devices to circuit modeling and integrated applications. After finishing this workshop, the participants will be able to execute the various analysis needed to characterize devices and circuits individually.

Total 40 students were registered for the workshop and participation certificate for all 40 issued by college.

Dr. Rajasekhar Turaka and Dr. Hariprasad Naik worked as Faculty Coordinators for the workshop.

Day-1:

After inaugural session Head of the Department addressed the gathering about the one-week workshop on hand-on training in VLSI Design.

Dr. Rajasekhar Turaka briefed out concepts such as VLSI design Technology, ASIC/FPGA design flow and architectural level optimization techniques such as pipelining, parallelism and retying. Post lunch session was hands-on Verilog HDL programming.

Day-2:

The day started with the concept of Adders, Multipliers and its applications in VLSI Design. After a small tea break, he explained the design procedure of 64-bit Adder & Subtractor with an example. Afternoon complete session was hands on training on Xilinx Vivado tool.

Day-3:

Third day was very interesting research issues in VLSI Design domain were discussed and after a small tea break, explained the design of 64-bit Vedic Multiplier and 64-bit Vedic Multiply and Accumulate (MAC) based on Vedic mathematics. Afternoon session was hands on training on design of 64-bit Arithmetic Logic Unit (ALU) using Verilog HDL and implemented on Xilinx Artix-7 board.

Day-4:

This day discussion was all about Back-end VLSI Design and CMOS Transistor level designs from scratch. After lunch, he explained the design procedure of basic CMOS circuits such as Inverter, 2-input NAND and NOR in Cadence Virtuoso tool.

Day-5:

The fifth day forenoon session was started with design of various Full Adders and also discussed about delay and power calculations. After lunch, hands on practice on the design of 14T Full Adder.

Day-6:

Day 6 talk was on the concepts of Array Multipliers in forenoon session and afternoon session various case studies were discussed.

In the valedictory session speakers were facilitated and a vote of thanks was presented by workshop coordinator.

Glimpse of the Workshop:


NALLA NARASIMHA REDDY
Education Society's Group of Institutions-Integrated Campus
(UGC AUTONOMOUS INSTITUTION)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
One Week Workshop on
Hands-on Training in VLSI Design
17-10-2022 to 22-10-2022
Venue : E-CAD Lab (S-2)
cadence


NALLA NARASIMHA REDDY
Education Society's Group of Institutions-Integrated Campus
(UGC AUTONOMOUS INSTITUTION)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
One Week Workshop on
Hands-on Training in VLSI Design
17-10-2022 to 22-10-2022
Venue : E-CAD Lab (S-2)
cadence


NALLA NARASIMHA REDDY
Education Society's Group of Institutions-Integrated Campus
(UGC AUTONOMOUS INSTITUTION)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
One Week Workshop on
Hands-on Training in VLSI Design
17-10-2022 to 25-10-2022
Venue : E-CAD Lab (S-2)
cadence
25