Report on

"Analog and Digital System Design Using Cadence EDA Tool"

(From 15th Dec 2015 – 19th Dec 2015)

Objective:

The aim of this Certificate Program is to provide hands-on experience on the state-of-the-art Cadence EDA tools for VLSI Design. The participants will have an exposure to the Circuit Design & Simulation, Layout, Physical Verification (DRC, LVS), and Extraction. The workshop includes practice sessions on the Cadence design and simulation tools (Virtuoso, Spectre, Assura and Incisive).

About Cadence:

Cadence is a leading provider of EDA and semiconductor IP. Our custom/analog tools help engineers design the transistors, standard cells, and IP blocks that make up SoCs. Our digital tools automate the design and verification of giga-scale, giga-hertz SoCs at the latest semiconductor processing nodes. Our IC packaging and PCB tools permit the design of complete boards and subsystems. Cadence also offers a growing portfolio of design IP and verification IP for memories, interface protocols, analog/mixed-signal components, and specialized processors. And reaching up to the systems level, Cadence offers an integrated suite of hardware/software co-development platforms. In short, Cadence® technology helps customers build great products that connect the world.

Certificate Program Topics:

- Introduction to VLSI, Technologies, Applications, Future Trends in VLSI.
- Design and Analysis of Analog Circuits.
- Design and Analysis of Digital Circuits.
- Design of Layouts of Analog and Digital Circuits.

Registration Details:

- Prior registration for the workshop by submitting the duly filled registration form is mandatory on or before December 01, 2015.
- Registration Form & Registration Process is available at Registration Page.
- Registration fee for attending the workshop is Rs.300/ per student.

Certificate Program Process:

The program involves individual and group exercises as well as input from the course leader, and presentations from the speakers. There were many opportunities to raise questions or concerns throughout the Workshops.

The following approaches were used

- Lectures
- Discussions
- Group work which constituted a means for developing the skills of participants.
- Practice sessions

Day-1:

The Certificate Program session started at 10:00am with a brief lecture on history and invention of transistors, IC's integration to VLSI technology, VLSI design flow, VLSI Design Styles, the design issues and design methodologies followed by Trends and future scope in VLSI.

The session started by giving an introduction to different EDA Tools and discussed the importance of Cadence EDA tool. There after tool was introduced to the participants with the design of basic inverter and then the students have simulated the circuit using spectre and done different analysis transient, DC, AC etc. Also the participants have observed the characteristics of transistors by changing different parameters like W/L ratios and variations in biasing the circuit etc.

Day-2 & Day-3:

The session started with a lecture on fundamentals of analog signals and system, and the design and analysis of different analog circuit. Followed by the design entry in virtuoso (Schematic editor).

In this session the students have simulated the circuit using spectre and done different analysis transient, DC, AC etc. Also the participants have observed the characteristics of transistors by changing different parameters like W/L ratios and variations in biasing the circuit etc.

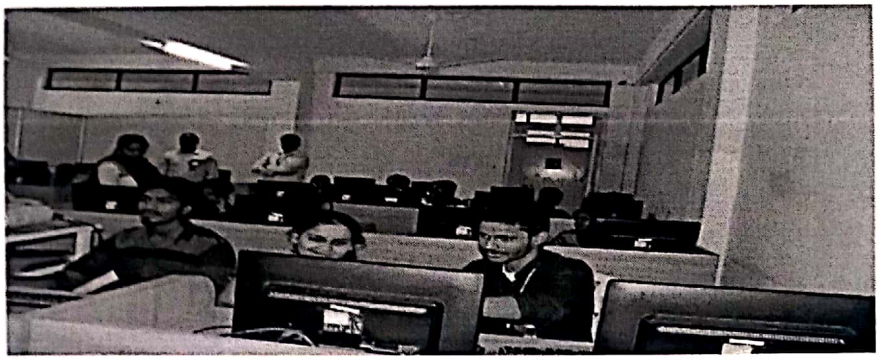
Day-4 & Day-5:

The session was started by introducing the Custom IC Flow, and the design rules for 180nm technology, followed by the introduction to stick diagrams and Layouts. And the participants have done the layout for an inverter without design violations.

This session was dedicated for LVS and RC extraction and followed by the post layout simulation of inverter. After layout simulation the results are compared with the schematic results.

Certificate Program Conclusions

The key issues of the workshop were summarized and the workshop was closed on October 30, 2016 with concluding remarks from the Dean school of Enginerring, NNRG Dr. G.Janardhana Raju, ECE HOD Mr. P.S.sreenivasa Reddy, and workshop conveners Ms. Samarla Shilpa, Ms. Sneha Talari, Mr.S. Srinivasa Rao and N.Kurumaiah Assistant Professors, ECE Department.



Practice Session on "Analog and Digital System Design Using Cadence EDA Tool".

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