Profile of Dr. C.V.Krishna Reddy

Designation: Director

Institution: Nalla Narasimha Reddy Education Society's Group of Institutions-Integrated Campus (UGC Autonomous Institution), Hyderabad

Educational Qualifications:

1. B.Tech (Electronics& Communication Engineering) , RVR&JC College of Engineering, Nagarjuna University, Guntur, AP; Passed in First class with 64.2% in 1989
2. M.E.(Applied Electronics), PSG College of Technology, Bharathiayar University, Coimbatore, Tamil Nadu; Passed in First class with 78% in 1997
3. PhD(ECE- VLSI Design) , J N T University, Hyderabad, TS; 2008

Professional Memberships: Fellow IETE, SM IEEE, MISTE

Employment Details :

Organization	Position	Duration	
Nalla Narasimha Reddy Education Society's Group of Institutions(NNRG) Hyderabad	Director	02-09-2011	Till date
Nalla Narasimha Reddy Education Society's Group of Institutions, Hyderabad	Dean	01-07-2010	01-09-2011
VSM Engineering College, Hyderabad	Principal	25-05-2008	30-04-2010
Kakatiya Institute of Technology, Warangal	Associate Professor	28-02-1998	24.05.2008
Vellore Engineering College, Vellore, TN (Present VIT)	Sr. Lecturer	9-5-1997	27 -2-1998
BLDEA's College of Engineering Bijapur, Karnataka	Lecturer	16-7-1990	6-5- 1997

Administrative Assignments:

1. Director NNRG (Engineering, Pharmacy, MBA) 2011-Till date
2. Dean NNRG(School of Engineering) 2010-2011
3. Principal VSM Engineering College, Hyderabad 2008-2010
4. Head of the Department(ECE) KITS, Warangal 2003-2008
5. Chairman, IETE Warangal Center 2007-2011
6. Hon Secretary, IETE Warangal Center/Sub center 2003-2007

Research Experience:

Area of Interest: VLSI Design, Embedded Design, Signal Processing
PhD Guidance:
Registered : 3
Submitted : 1

Publications:

Sl. No.	Titlewith page No	Journal name publications	ISSN No.	Journal type	International/ National
1	**A novel design of full adder cell for VLSI applications, vol. 109, issue 5,4/2022**	International Journal of Electronics, Tailor& Francis	13623060, 00207217	SCI	International
2	Performance Of Leakage Power Minimization Technique For CMOS VVLSI Technology-670-683, 10/2021	Journal of Tianjin University Science and Technology,	0493-2137	Scopus	International
3	Design Of Level Shifter For Low Power Application 75-88, 10/2021	Journal of Jilin University (Engineering and Technology Edition)	1671-5497	Scopus	International
4	Analysis Of Software Power Consumption Of Embedded DSP Software 115-127, 10/2021	Journal of Xi'an Shiyou University, Natural Sciences Edition	1673-064X	Scopus	International
5	Algorithm for auto correction in digital VLSI circuits 4922-4933, 2021	Design Engineering,	0011-9342	Scopus	International
6	Implementation Of Sobol Sequence Pattern Generator Based MBIST vol. 55, no. 1(11), pp. 111-116, 2021	Journal of the Maharaja Sayajirao University of Baroda, 2021	0025-0422	UDC care	National
7	Chip Design For Video Compression System Using Real-Valued Discrete Wavelet Transform pp. 169-174, 2021.	The Journal Of Oriental Research Madras,10/2021	0022-3301	UGC care	National
8	Implementation of Low Power Differential Voltage-Controlled Oscillator using CNTFET Technology vol. 8, no. 5, pp. 4146-4156, 2019	International Journal of Research,	2236-6124	UGC care	International
9	Implementation of Area and Power Efficient Mixed Logic Line Decoders using MGDI Technology vol. 5, no. 2, pp. 544-552, 2016	International Journal of Research,7/2017	2236-6124	UGC care	International
10	Implementation of Digital Integrated Circuit for Radio Frequency to DC Power Converter vol. 5, no. 1, pp. 947-955,	**Journal of Applied Science and Computations**	1076-5131	UGC care	International
11	Implementation of Nano Calculator using Advanced QCA based Majority Logic Formulations vol. 6, no. 12, pp. 292-300,	International Journal of Research 12/2017	2236-6124	UGC care	International
12	Design of PLL-Independent LC Oscillator with High Efficiency for Communication Applications	Journal of Applied Science and Computations, 1/2017	1076-5131	UGC care	International

13	Implementation of Area, Power Efficient Image using Multi-Level Block Truncation Coding with Fuzzy Decisions	International Journal of Research	2236-6124	UGC care	International
14	Design of STT-RAM cell in 45nm hybrid CMOS/MTJ,Vol.3 Issue 3, May-June2014 Pp 49-52	Int. Jou. of Science and Engg Applications	2319-7560		**International**
15	An Alternative Logic Approach to Implement Energy Efficient 90-Nm CMOS full adders. Vol 2 Issue 10 Oct 2013,Pp 70-73	Int. Jou of Scientific research	2277-8179		**International**
16	Design of an Efficient Reversible Logic Based Bidirectional Barrel shifter. Vol-2,3,4, 2012, p.p.No. 48-53.	International Journal of Electronics Signals and systems (IJESS)	2231-5969		**International**
17	Optimum Decimation and Filtering for reconfigurable Sigma Delta ADC Volume 11, Issue2 Dec 2013Pp101 - 111	Far East Journal of Electronics and Communications	0973-7006		**International**
18	An Alternative Logic Approach to Implement Energy Efficient 90-nM CMOS Full Adders Vol. 2Oct 2013 Pp 1-3	International Journal of Scientific Research(IJSR)	2277-8179		**International**
19	An Improved Optimization Techniques for Parallel Prefix Adder using FPGA Techniques for Parallel Prefix Adder using FPGA Vol. 3, Issue. 5, Sep - Oct. 2013 pp-3107-3115	International Journal of Modern Engineering Research (IJMER)	ISSN: 2249-6645		**International**
20	A Novel Architecture of LUT Design Optimization for DSP Applications Vol.-1, Issue-22012 p.p No 1-6	International Journal of Advanced Electrical and Electronics Engineering	2278-8948		**International**
21	Analysis on Digital Implementation of Sigma-Delta ADC with passive analog components. Vol. 2 2013 Pp 71-77	International Journal of Computing and Digital systems: ISSN	2210-142X		**International**
22	Design and Simulation of Voltage to Current Converter. Vol. 1, No.2 , July 2007	Technology Spectrum, Journal of JNTU			National
23	Design of Low power high speed segmented DAC. Vol..2, No.3 June 2008	Technology Spectrum, Journal of JNTU			National
24	Design and Simulation of Differential Mode CMOS Voltage to Current Converter Vol. 7, NO.3 Sept2007 pp. 220-224	LE Journal of Laboratory experiments			National
25	Power Optimization in Flash ADCs. Vol..No.3,2008	Far East International Journal of EC	0973-7006		**International**

Courses/FDPs Attended:

Name of the Course / FDP Attended	Place	Duration	Sponsoring Agency
NBA Accreditation and Teaching & learning in Engineering(NATE)	NPTEL (Online)	12 weeks	NPTEL, MHRD
Intellectual property Intelligence &Patent Drafting	NNRG , Hyderabad	17th -22nd Dec 2018(1 week)	AICTE -ISTE
Aspects of IC Design	NIT Warangal	8- 17th February, 2019(1	Electronics & ICT

		Week)	Academy &NITW
Analog CMOS VLSI Design using Cadence Tools, from	Entuple, Bangalore	7- 11th Dec 2015.(1 week)	Organized by Entuple, Bangalore
DSP Tools and Practice	IIT, Kharagpur	12-17th June, 2006(1 week)	IIT, Kharagpur
DSPAA at NIT, Warangal,.	NIT, Warangal	22nd Mar- 2nd Apr, 2004(2 Week)	AICTE-ISTE
VLSI system Design	REC Warangal	23July-4th Aug 2001(2 Week)	AICTE -ISTE
High speed Networking	REC, Warangal,	4th- 15 October, 1999.(2 week)	AICTE-ISTE

The information given above is true to the best of my Knowledge.

C V Krishna Reddy