NALLA NARASIMHA REDDY EDUCATION SOCIETY'S GROUP OF INSTITUIONS

(UGC AUTONOMOUS INSTITUTION)

M.TECH. IN EMBEDDED SYSTEMS & VLSI

COURSESTRUCTURE ANDSYLLABUS

(R24 Regulations)
Applicable from AY 2024-25Batch

I Year I Semester

S.No.	Course Code	Course Title	L	T	P	Credits
1.	Professional Core – I	Digital System Design with FPGAs	3	0	0	3
2.	Professional Core – II	ARM Microcontrollers	3	0	0	3
3.	Professional Elective – I	1. Pattern Recognition and Machine Learning 2. Embedded Sensors 3. Memory Technologies	3	0	0	3
4.	Professional Elective – II	1. Embedded Real Time Operating Systems 2. Advanced Computer Architecture 3. Communication Buses & Interfaces	3	0	0	3
5.	Lab – I	Digital System Design with FPGAs Lab	0	0	4	2
6.	Lab – II	ARM Microcontrollers Lab	0	0	4	2
7.		Research Methodology & IPR	2	0	0	2
8.	Audit – I	Audit Course – I	2	0	0	0
		Total	**16**	**0**	**8**	**18**

I Year II Semester

S.No.	Course Code	Course Title	L	T	P	Credits
1.	Professional Core – III	CMOS Analog IC Design	3	0	0	3
2.	Professional Core – IV	System Design with Embedded Linux	3	0	0	3
3.	Professional Elective – III	1. IoT Architectures and System Design 2. SOC Design 3. Design For Testability	3	0	0	3
4.	Professional Elective – IV	1. Device Modelling 2. Secure Networks 3. Physical Design Automation	3	0	0	3
5.	Lab – III	CMOS Analog IC Design Lab	0	0	4	2
6.	Lab – IV	System Design with Embedded Linux Lab	0	0	4	2
7.		Mini Project with Seminar	0	0	4	2
8.	Audit – II	Audit Course- II	2	0	0	0
		Total	**14**	**0**	**12**	**18**

II YEAR I SEMESTER

S.No.	Course Code	Course Title	L	T	P	Credits
1.	Professional Elective – V	1. CMOS Mixed Signal Design 2. Embedded Networks 3. Nano Materials and Nano Technology	3	0	0	3
2.	Open Elective	Open Elective	3	0	0	3
3.	Dissertation	Dissertation Work Review – II	0	0	12	6
		Total	**6**	**0**	**12**	**12**

II YEARIISEMESTER

S.No.	Course Code	Course Title	L	T	P	Credits
1.	Dissertation	Dissertation Work Review – III	0	0	12	6
2.	Dissertation	Dissertation Viva-Voce	0	0	28	14
		Total	**0**	**0**	**36**	**20**

Open Electives:

1. Business Analytics
2. Industrial Safety
3. Operations Research
4. Cost Management of Engineering Projects
5. Composite Materials

Audit Course I & II:

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development Through Life Enlightenment Skills

DIGITAL SYSTEM DESIGN WITH FPGAs (PC – I)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Prerequisite: Switching Theory and Logic Design

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To expose the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands Test Pattern Generation Techniques for Fault detection.
4. To design fault diagnosis in Sequential circuits.
5. To understand in the design of flow using case studies.

UNIT -I

Programmable Logic Devices: The concept of Programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA Technology, Architecture, Virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT -II

Analysis and derivation of clocked sequential circuits with state graphs and tables: Sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for Sequential circuits, Design of a Sequence detector, More complex design problems, Guidelines for construction of State graphs, serial data conversion, Alphanumeric state graph notation. Need and design strategies for multi-clock Sequential circuits. [TEXTBOOK-2]

UNIT –III

Sequential circuit Design: Design procedure for Sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a Comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and Testing of Sequential circuits, Overview of Computer Aided Design. [TEXTBOOK-2]

UNIT –IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault Detection & Redundancy, Fault equivalence and Fault location, Fault dominance, Single stuck at Fault model, Multiple Stuck at Fault models, Bridging Fault model. Fault diagnosis of Combinational circuits by conventional methods, Path sensitization techniques, Boolean Difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random Testing, Transition count testing, Signature analysis and test bridging Faults. [TEXTBOOK-3 & Ref.1]

UNIT – V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State Identification and Fault detection experiment, Machine identification, Design of Fault detection experiment. [Ref.3]

TEXT BOOKS:

1. Digital Electronics and Design with VHDL- Volnei A. Pedroni, Elsevier Science, 2008.
2. Fundamentals of Logic Design-Charles H.Roth, Jr. -5th Ed., Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C. LEE, PHI, 2008.

REFERENCE BOOKS:

1. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using Programmable Logic Devices- Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory - ZviKohavi&Niraj K. Jha, 3rd Edition, Cambridge, 2010.

ARM MICROCONTROLLERS (PC - II)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Prerequisite: Microprocessors and Microcontrollers

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completion of this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT- I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, Floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, Memory map, Stack memory, Memory Protection Unit (MPU), Exceptions and Interrupts-what are exceptions, Nested Vectored Interrupt Controller(NVIC), Vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT - II

Introduction to the ARM Instruction Set: Data processing instructions, Branch instructions, Load-store instructions, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT- III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and Cortex M4 processors-Processor type, Processor architecture, Instruction set, Block diagram, Memory system, Interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors- Performance, Code density, Low power, Memory system, Memory protection unit, Interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT- IV

Instruction Set of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, Understanding the Assembly Language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in programming.

UNIT- V

Floating Point operations about Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- Overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU->FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP applications: DSP on a Microcontroller, Dot product example, Writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT- ARM System Developer's Guide Designing and Optimizing System Software, Elsevier Publications, 2004.
2. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber - Arm System on Chip Architectures –Edison Wesley, 2000.
2. David Seal - ARM Architecture Reference Manual, Edison Wesley, 2000.

PATTERN RECOGNITION AND MACHINE LEARNING (PE - I)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Prerequisite: Statistics and Linear Algebra

Course objectives:

1. The student will be able to understand the mathematical formulation of patterns.
2. To study the various linear models.
3. Understand the basic classifiers.
4. Can able to distinguish different models.

Course Outcomes: On completion of this course student will be able to

1. Familiar with the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods.
4. Design the Markov and Mixed models.

UNIT - I

Introduction to Pattern recognition: Mathematical Formulation and basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Non-parametric design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass generalization.

UNIT - II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares, Sequential learning, Regularized least squares, Multiple outputs, The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT - III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification

UNIT - IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a Chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

UNIT - V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An alternative view of EM Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer, 2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009.

EMBEDDED SENSORS (PE - I)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

UNIT - I

Introduction to sensors: Sensors, Sensors Classification, Sensor Characteristics –Sensors for Mobile Communication devices, Accuracy, Calibration error, Hysterisis, Non-linearity, Saturation, Repeatability, Resolution, Special properties, Excitation, Dynamic Characteristics, Dynamic Models of Sensor Elements, Environmental factors, Reliability, Application Characteristics.

UNIT - II

Analog sensors: Potentiometric Sensors, Piezoresistive Sensors, Capacitive Sensors, Inductive and magnetic Sensors – Transverse inductive Sensors, Magneto resistive Sensors, Optical Sensors, Electromagnetic Sensors, Cariolis mass flow Sensor, Semiconductor PN junction Sensor, Optical temperature Sensors, Thermal Sensors, Electrical and Electrochemical Sensors.

UNIT - III:

Digital sensors: Digital Sensors for Temperature, Pressure, Moisture, Accelerometers, Inclinometers, Gyroscopes, Flex, Color, Light, Programming timers, Frequency Counters, PWM generation, Demodulation.

UNIT - IV

Thermometric and optical sensors: Sensors with Thermistors and Pellistors, Pyroelectric Sensors, Sensors based on Thermal effects, Optical fibers as a basis for Optical Sensors, Fiber Sensors without chemical receptors, Optodes: Fiber Sensors with a chemical receptor, Optodes with simple receptor layers, Optodes with complex receptor layers, Pressure Sensors.

UNIT - V

Detectors of humans: Ultrasonic detectors, Microwave motion detectors, Optoelectronic motion detectors, Optical presence sensors, Pressure gradient sensors, 2D pointing devices, Gesture sensing, Tactile Sensors.

TEXT BOOKS:

1. Jacob Fraden, “Hand book of Modern Sensors: Physics, Designs and Applications”, 2014, 4th ed., Springer, New York.
2. Sergey Y. Yurish, “Digital Sensors and Sensor Systems: Practical Design”, 2011, 1st ed., IFSA publishing.

REFERENCE BOOKS:

1. Peter Grundler, “chemical sensors- An introduction for scientists and engineers”, springer publications
2. Gregory T.A. Kovacs “Micromachine Transducers” source book 1st edition.
3. Chnag Liu “Foundation of MEMS” 2nd edition.
4. KouroshKalatar-zadeh, “Nanotechnology-Enabled Sensors” Springer publications (2007).

MEMORY TECHNOLOGIES (PE – I)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To know the RAM technologies, architecture and applications
2. To know the circuit design concepts of Non-volatile memories
3. To understand the Memory package density technologies.

Course Outcomes: At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know, how of the state-of-the-art memory chip design

UNIT - I

Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT - II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

UNIT - III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT - IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices.

UNIT - V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXT BOOKS:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. KiyooItoh, “VLSI memory chip design”, Springer International Ed.

REFERENCE BOOKS:

1. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI

EMBEDDED REAL TIME OPERATING SYSTEMS (PE – II)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Prerequisite: Computer Organization and Operating System

Course Objectives:

1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes: Students will be able to:

1. Explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Describe how a real-time operating system kernel is implemented.
3. Explain how the real-time operating system implements time management.
4. Work with real time operating systems like RT Linux, Vx Works, MicroC /OS-II, Tiny OS

UNIT - I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, Tasks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

UNIT - III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

ADVANCED COMPUTER ARCHITECTURE (PE – II)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To understand the fundamental of computer design
2. To know the pipelines and parallelism concepts
3. To know the issues in interconnect networks

Course Outcomes: At the end of the course, students will be able to:

1. Familiarize the instruction set, memory addressing of Computer
2. Handle the issues in pipelining and parallelism
3. Familiarize the practical issues in inter network

UNIT - I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, Measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, Classifying instruction set- Memory addressing- type and size of operands, Operations in the instruction set.

UNIT - II

Pipelines: Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation. ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT - V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting Networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA- 64 ILP in Embedded and Mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", McGraw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

COMMUNICATION BUSES AND INTERFACES (PE - II)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To know how to select the suitable Buses for different applications
2. To know the architecture of CAN and applications
3. To understand the use of PCIe, USB etc.,
4. To know the serial communication protocol

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular Serial Bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto Serial Bus.
3. Design and develop peripherals that can be interfaced to desired Serial Bus.

UNIT - I

Serial Busses - Physical interface, Data and Control signals, Features, Limitations and applications of RS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, Applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, Applications

UNIT - IV

USB - Transfer types, Enumeration, Descriptor types and contents, Device driver

UNIT - V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and Copper cable

TEXT BOOKS:

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org, http://www.pcisig.com/www.pcisig.com, http://www.usb.org/www.usb.org

DIGITAL SYSTEM DESIGN WITH FPGAs LAB (Lab – I)

M.Tech. I Year I Sem

L	T	P	C
0	0	4	2

Part - I:

Programming can be done using any Complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using Pattern generator (32 channels) and Logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using Encoder (without and with parity).
5. Design of Combinational circuit using Multiplexer.
6. Design of 4 bit Binary to Gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, Comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any Sequence Counter
10. Design of a N- bit register of Serial- in Serial –out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment,

ARM MICROCONTROLLERS LAB (Lab – II)

M.Tech. I Year I Sem

L	T	P	C
0	0	4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

RESEARCH METHODOLOGY AND IPR

M.Tech. I Year I Semester

L	T	P	C
2	0	0	2

Course Objectives:

1. To understand the research problem
2. To know the literature studies, plagiarism and ethics
3. To get the knowledge about technical writing
4. To analyze the nature of intellectual property rights and new developments
5. To know the patent rights

Course Outcomes: At the end of the course, students will be able to:

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT - III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT - IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology.Patent information and databases.Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc.Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

CMOS ANALOG IC DESIGN (PC-III)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: Analog Electronics

Course Objectives: Analog circuits play a very crucial role in all Electronic systems and due to continued miniaturization; many of the Analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS Analog IC's.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all Analog CMOS IC's.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and Op-Amp's.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS Analog IC's.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various Amplifiers like differential, Current and Operational Amplifiers.

UNIT -I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current Mirror with Beta Helper, Degeneration, Cascode Current Mirror and Wilson Current Mirror, Current and Voltage References, Band Gap Reference.

UNIT –III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –IV

CMOS Operational Amplifiers: Design of CMOS and Op-Amp's, Compensation of and Op-Amp's, Design of Two-Stage and Op-Amp's, Power-Supply Rejection Ratio of Two-Stage and Op-Amp's, Cascode and Op-Amp's, Measurement Techniques of and Op-Amp's.

UNIT – V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

SYSTEM DESIGN WITH EMBEDDED LINUX (PC – IV)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To know the difference between Embedded Linux and Desktop Linux
2. To understand the Kernel concepts of Embedded Linux
3. To learn the debugging, writing, profile applications and drivers in Embedded Linux.

Course Outcomes: At the end of this course, students will be able to

1. Familiarity of the Embedded Linux Development Model.
2. Write, debug, and profile applications and drivers in Embedded Linux.
3. Create Linux BSP for a Hardware platform

UNIT -I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling. Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT -II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT –III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and Kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules

UNIT –IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT – V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds, “Mastering Embedded Linux Programming” - Second Edition, PACKT Publications Limited.
2. KarimYaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014

IOT ARCHITECTURES AND SYSTEM DESIGN (PE – III)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To know the definition and basic concepts of IoT
2. Learn the interfacing the IoT and M2M
3. To understand the Architecture of IoT

Course Outcomes: Students will be able to:

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

UNIT -I

IoT Introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT -II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The International driven global value chain and global information monopolies.

UNIT –III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT –IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack

UNIT – V

IoT System design: Challenges associated with IoT, Emerging pillars of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. SudipMisra, Anandarup Mukherjee, Arijit Roy “Introduction to IOT”, Cambridge University Press.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry “IoT Fundamentals Networking technologies, protocols, and use cases for IoT”, Cisco Press

REFERENCE BOOKS:

1. Cunopfister, “Getting started with the internet of things”, O Reilly Media, 2011
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1 st Edition, Apress Publications.
3. “Internet of Things concepts and applications”, Wiley
4. ArshdeepBahga,VijayMadisetti “Internet of Things A Hands on approach”, Universities Press
5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, “Internet of things” John Wiley and Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/Maker Media Publishers.

SOC DESIGN (PE – III)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To learn ASIC design concepts and strategies
2. To know the NISC applications and advantages
3. To familiar with simulation and synthesis process

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for Engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT -I

ASIC: Overview of ASIC types, Design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC Design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT -II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- Set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, Modeling NISC architectures and systems, Use of Generic Netlist Representation - A formal language for specification, Compilation and synthesis of Embedded processors.

UNIT –III

Simulation: Different simulation modes, Behavioural, Functional, Static timing, Gate level, Switch level, Transistor/circuit simulation, Design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, Clock tree design issues.

UNIT –IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, Clock gating, Adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), Building block Optimization, Building block memory, Power down techniques, Power consumption verification.

UNIT – V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, Trails paths, Connectivity, Components, Mapping/visualization, Nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, Optimization constraints, Synthesis report, Analysis Single core and Multi core systems, Dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006

REFERENCE BOOKS:

1. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

DESIGN FOR TESTABILITY (PE – III)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Digital System Design

Course Objectives:

1. To acquire the knowledge of fundamental concepts of testing
2. To provide broad understanding the Fault simulation.
3. To illustrate the framework of Built-in-self test and Boundary scan methods.

Course Outcomes: Students will be able to

1. Acquire verification knowledge and test evaluation
2. Design for testability rules and techniques.
3. Utilize the scan architectures for different digital circuits.
4. Acquire the knowledge of design of built-in-self test.

UNIT -I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT –III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT –IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT – V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

DEVICE MODELLING (PE –IV)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To obtain the functional relationship among the terminal electrical variables of the device that is to be modeled
2. To know the physical properties of materials and devices
3. To know the MOS transistor low frequency model
4. To understand the characteristics of the FinFETs and its applications

Course Outcomes: Students will be able to

1. Develop a functional relationship among the terminal electrical variables of the device that is to be modeled.
2. Describe the behavior of all components successfully
3. Perform the simulation and analyze the VLSI circuits
4. Use the FinFET for various applications

UNIT -I

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.

UNIT -II

MOS Capacitor Characteristics and Non idealities: CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, Oxide fixed charges, Interfacial charges.

UNIT –III

The MOS transistor: Small signal modeling for Low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

UNIT –IV

The bipolar transistor: Eber's-Moll model; charge control model; Small-signal models for Low and High frequency and switching characteristics.

UNIT – V

FinFETs: I-V characteristics, Device capacitances, Parasitic effects of extension regions, Performance of simple combinational gates and amplifiers, Novel circuits using FinFETs and GAA devices.

TEXT BOOKS:

1. S. M. Sze, "Physics of Semiconductor Devices", 2nd Ed., Wiley Eastern, 1981.
2. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill, 1987.
3. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press, 1995.
4. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer. 2009

SECURE NETWORKS (PE-IV)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To underlying principles and techniques for network and communication security.
2. To learn practical examples of security problems and principles for counter measures
3. To provide cryptographic methods, protocols and applications.

Course Outcomes: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT -I

Security: Need, Security services, Attacks, OSI Security Architecture, One time passwords, Model for Network security, Classical Encryption Techniques like substitution Ciphers, Transposition Ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT -II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT –III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream Cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT –IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, Hash functions, Message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT – V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, Viruses, Trojans, Virus Counter measures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:

1. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

PHYSICAL DESIGN AUTOMATION (PE -IV)

M.Tech. I Year II Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To understand the concepts of Physical Design Process (Partitioning, Floor planning etc.,)
2. To know the concepts of design optimization algorithms and their application
3. To understand the clock and power design concepts

Course Outcomes: At the end of the course, students will be able to:

1. Implement automation process for VLSI System design.
2. Familiarize to use various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

UNIT -I

Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT -II

Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, Delay models, Layout styles.

UNIT –III

Placement: Problem formulation, Classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT –IV

Global routing: Problem formulation, Classification of global routing, Maze routing algorithms, Line-Probe algorithms, Shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.

Detailed Routing: Problem formulation, Classification, Single layer, Two layer, Three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT – V

Over the Cell Routing - Single layer and Two-layer routing: Over the cell routing, Two layer, Three layer and Multi-Layer OTC Routing.

Via Minimization: Constraint and Unconstrained via minimization.

Clock and Power Routing: Clocking schemes, Design considerations for the clock, Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley& Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

CMOS ANALOG IC DESIGN LAB (Lab – III)

M.Tech. I Year II Sem

L	T	P	C
0	0	4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Design Analog Circuit using CMOS.
2. Use EDA tools like Cadence, Mentor Graphics and other Open source software tools like Ngspice

List of Experiments:

1) Use VDD = 1.8V for 0.18 um CMOS process, VDD = 1.3V for 0.13 um CMOS Process and VDD = 1V for 0.09 um CMOS Process.
   a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
   c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
   d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel Length Modulation factor.
   e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30 mV
      To extract Vth use the following procedure.
      i. Plot gmvs VGS using NGSPICE and obtain peak gm point.
      ii. Plot y= ID/(gm)1/2 as a function of VGS using Ngspice.
      iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

   Tabulate your result according to technologies and comment on it.
2) Use VDD = 1.8V for 0.18 um CMOS process, VDD =1.2V for 0.13 um CMOS Process and VDD = 1V for 0.09 um CMOS Process.
   a) Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload =50 fF)
   c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012 pF, Cload = 4pF, Rload = k)
3) Use Ngspice to build a three stage and five stage Ring Oscillator circuit in 0.18 um and 0.13 um technology and compare its frequencies and time period.
4) Perform the following
   a) Draw small signal voltage gain of the minimum-size inverter in 0.18 um and 0.13 um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18 um and 0.13 um process.

b) Consider a simple CS Amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18 um technology. (W/L) MN=5, (W/L) MP=10 and L= 0.5 um for both transistors.
   i. Establish a test bench, as explained in the lecture, to achieve VDSQ = VDD/2.
   ii. Calculate input bias voltage if bias current = 50 uA.
   iii. Use Ngspice and obtain the bias current. Compare its value with 50 uA.
   iv. Determine small signal voltage gain, - 3 dB BW and GBW of the Amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
   v. Plot step response of the Amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
   Vi. Use Ngspice to determine input voltage range of the Amplifier

5) Three OP-AMP INA. Vdd = 1.8V Vss = 0V, CAD tool: Mentor Graphics DA.
Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OP-AMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
   i. Draw the schematic of Op-Amp macro model.
   ii. Draw the schematic of INA.
   iii. Obtain parameters of the Op-Amp macro model such that
      a. low-frequency voltage gain =5 x 104,
      b. unity gain BW (fu) =500 KHz,
      c. input capacitance = 0.2 pF,
      d. output resistance =,
      e. CMRR=120 dB
   iv. Draw schematic diagram of CMRR simulation setup.
   v. Simulate CMRR of INA using AC analysis (it's expected to be around 6 dB below CMRR of OP-AMP).
   vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
   vii. Repeat (iii) to (vi) by considering CMRR of all OP-AMPs to be 90 dB.

6) Technology: UMC 0.18 um, VDD=1.8V. Use MAGIC or Microwind.
   a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
   b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
   c) Use extracted netlist and obtain tPHL, tPLH for the middle inverter using Eldo.
   d) Use interconnect length obtained and connect the second and third inverter.
   Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’

SYSTEM DESIGN WITH EMBEDDED LINUX LAB (Lab – IV)

M.Tech. I Year II Sem

L	T	P	C
0	0	4	2

List of Experiments:

1. **Functional Testing of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.

2. **Exporting Display on to Other Systems:** Making use of available Laptop/Desktop displays as a display for the device using SSH client & X11 display server.

3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.

4. **Interfacing Chronos eZ430:** Chronos device is a programmable Texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.

5. **ON/OFF Control Based on Light Intensity:** Using the light sensors, Monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined Threshold light intensity value.

6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)

7. **Dice Game Simulation:** Instead of using the conventional Dice, Generate a random value similar to Dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double Dice game.

8. **Displaying RSS News Feed on Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like Twitter or other information websites. Python can be used to acquire data from the internet.

9. **Porting Open wrt to the Device:** Attempt to use the device while connecting to a wi-fi network using a USB dongle and at the same time providing a wireless access point to the dongle.

10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.

11. **Webcam Server:** Interfacing the regular USB webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. **FM Transmission:** Transforming the device into a regular FM Transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

CMOS MIXED SIGNAL DESIGN (PE - V)

M.Tech. II Year I Semester

L	T	P	C
3	0	0	3

Pre-Requisites: Analog Electronics

Course Objectives: The objectives of this course are to

1. Introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these building blocks.
3. Understand design and operation of basic Analog circuits.
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes: At the completion of this course, each student will have demonstrated proficiency in:

1. Designing CMOS Analog circuits to achieve performance specifications.
2. Analyzing CMOS based switched capacitor circuits.
3. Designing data converters and know how to use these in specific applications
4. Design a mixed-signal circuit with understanding design flow.

UNIT -I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- Basic building blocks, Operation and Analysis, Non- ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, Bi-quad filters.

UNIT -II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, Applications

UNIT –III

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT –IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT – V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi-bit quantizers, Delta sigma D/A.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013.

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

EMBEDDED NETWORKS (PE – V)

M.Tech. II Year I Semester

L	T	P	C
3	0	0	3

Pre-Requisites: Computer Networks.

Course Objectives:

1. To elaborate on the conceptual frame work of physical layer and topological issues of networking in Embedded Systems.
2. To emphasis on issues related to guided and unguided media with specific reference to Embedded device level connectivity.

Course Outcomes: Student will be able to:

1. Acquire knowledge on communication protocols of connecting Embedded Systems.
2. Master the design level parameters of USB and CAN Bus protocols.
3. Design Ethernet in Embedded networks considering different issues.
4. Acquire the knowledge of wireless protocols in Embedded domain.

UNIT -I

Embedded Communication Protocols: Embedded Networking: Introduction, Serial/Parallel Communication, Serial communication protocols, RS232 standard, RS485, Synchronous Serial Protocols, Serial Peripheral Interface (SPI), Inter Integrated Circuits (I2C), PC Parallel port programming, ISA/PCI Bus protocols, Firewire.

UNIT -II

USB and CAN Bus: USB bus – Introduction, Speed Identification on the bus, USB States, USB bus communication Packets, Data flow types, Enumeration, Descriptors, PIC 18 Microcontroller USB Interface, C Programs, CAN Bus – Introduction, Frames, Bit stuffing, Types of errors, Nominal Bit Timing, PIC microcontroller CAN Interface, A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network, Inside Ethernet, Building a Network: Hardware options, Cables, Connections and network speed, Design choices: Selecting components, Ethernet Controllers, Using the internet in local and internet communications, Inside the Internet protocol.

UNIT –IV

Embedded Ethernet: Exchanging messages using UDP and TCP, Serving web pages with Dynamic Data, Serving web pages that respond to user Input, Email for Embedded Systems – Using FTP, Keeping Devices and Network secure.

UNIT – V

Wireless Embedded Networking: Wireless sensor networks – Introduction, Applications Network Topology, Localization, Time Synchronization, Energy efficient MAC protocols, SMAC, Energy efficient and robust routing, Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari, Cambridge press 2005.

NANOMATERIALS AND NANOTECHNOLOGY (PE – V)

M.Tech. II Year I Semester

L	T	P	C
3	0	0	3

Course Objectives:

1. To know the characteristics of Nano materials and their utility
2. To understand the basic science behind the design and fabrication of Nano scale systems.
3. To know the basic principle of working of MEMS and its applications

Course Outcomes: At the end of the course, students will be able to:

1. Formulate new engineering solutions for current problems and competing technologies for future applications.
2. Made inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
3. Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems

UNIT -I

Introduction of Nano materials and nanotechnologies, Features of nanostructures, Applications of Nano-materials and technologies, Nano dimensional Materials 0D, 1D, 2D structures , Size Effects, Fraction of Surface Atoms, Specific Surface Energy and Surface Stress, Effect on the Lattice Parameter, Phonon Density of States, the General Methods available for the Synthesis of Nanostructures, Precipitative, reactive, Hydrothermal/solvo thermal methods, Suitability of such methods for scaling , Potential Uses.

UNIT -II

Fundamentals of Nano-materials, Classification, Zero-dimensional Nano-materials, One-dimensional, Nano-materials, Two-dimensional Nano-materials, Three dimensional Nano-materials, Low-Dimensional Nano-materials and its Applications, Synthesis, Properties, and Applications of Low-Dimensional Carbon-Related Nano-materials.

UNIT –III

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding, Introduction to Nano Phonics.

UNIT –IV

CNTs: Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT’s, Multi-walled Nano-tubes, Single-walled Nano-tubes, Optical properties of CNT’s, Electrical transport in perfect Nano-tubes, Applications as case studies, Synthesis and Applications of CNT's.

UNIT – V

Ferroelectric materials, coating, molecular electronics and Nano-electronics, Biological and environmental, Membrane based application, Polymer based application.

TEXT BOOKS:

1. I Gusev and A ARempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1 st Indian edition by Viva Books Pvt. Ltd. 2008.
2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGraw Hill Education 2012.

REFERENCE BOOKS:

1. Kenneth J. Klabunde and Ryan M. Richards, “Nanoscale Materials in Chemistry”, 2 edition, John Wiley and Sons, 2009.
2. Bharat Bhushan, “Springer Handbook of Nanotechnology”, Springer, 3rd edition, 2010.
3. Kamal K. Kar, “Carbon Nanotubes: Synthesis, Characterization and Applications”, Research Publishing Services; 1 st edition, 2011, ISBN-13: 978-9810863975.