



NALLA NARASIMHA REDDY

Education Society's Group of Institutions - Integrated Campus
(Affiliated to JNTU Hyderabad, Approved by AICTE)
Academic Partnering with **ORACLE** ACADEMY



Dr. C. V. Krishna Reddy, M.E, Ph.D.

Director, NNRG

Education Qualifications:

- Ph. D. (ECE) from JNTU, Hyderabad in 2008.
- M. Tech (Applied Electronics) from PSG College of Tech., Bharathiyar university ,Coimbatore in 1996
- B. Tech (ECE) from RVR&JC College of Engineering (N. U), Guntur in 1989

Administrative Assignments:

- **Director**, Nalla Narasimha Reddy Education Society's Group of Institutions, Hyderabad from Sept 2011 to till date
- Council member IETE (co-opted) from 2012 to 2014
- **Dean**, School of Engineering, Nalla Narasimha Reddy Education Society's Group of Institutions, Hyderabad from July 2010 to Aug 2011
- **Chairman IETE Warangal**, Sub Centre from 2008- 2010
- **Principal**, VSM Engineering College, Hyderabad from May 2008 to April 2010

- **Head** of ECE dept , KITS Warangal from April 2005 to May2008
- **Chairman** , Board of Studies ECE , Kakatiya University, Warangal-2007-2008
- **Honorable Secretary IETE Warangal** Sub Centre from 2003-2008
- **Member**, Board of Studies EIE, ECE, Kakatiya University , 2003-2007

Papers Published:

- Dr. C V Krishna Reddy, **Design of STT-RAM cell in 45nm hybrid CMOS/MTJ**, IJSEA, Volume 3 Issue 3 May-June 2014.
- Dr. C V Krishna Reddy, **Optimum Decimation and Filtering for reconfigurable Sigma Delta ADC**, Far East IJEC, Volume 11 Issue 2 December 2013.
- Dr. C V Krishna Reddy, **An Alternative Logic Approach to Implement Energy Efficient 90-Nm CMOS full adders**, IJSR, Volume 2 Issue 10 October 2013.
- Dr. C V Krishna Reddy, **An Improved Optimization Techniques for Parallel Prefix Adder using FPGA Techniques for Parallel Prefix Adder using FPGA**, IJMER, Volume 3 Issue 5 September-October 2013.
- Dr. C V Krishna Reddy, **Analysis on Digital Implementation of Sigma-Delta ADC with passive analog components**, IJCDS, 2013.
- Dr. C V Krishna Reddy, **Design and Implementation of Reversible Logic Based Bidirectional Barrel Shifter**, IEEE-ICSE, 2012.
- Dr. C V Krishna Reddy, **Design of an Efficient Reversible Logic Based Bidirectional Barrel shifter**, IJESS, Volume 2 Issue 2,3,4 2012.
- Dr. C V Krishna Reddy, **A Novel Architecture of LUT Design Optimization for DSP Applications**, IJAEEE, Volume 1 Issue 2 2012.
- Dr. C V Krishna Reddy, **Power Optimization in Flash ADCs**, Far East IJEC, December 2008.
- Dr. C V Krishna Reddy, **Design of Low power high speed segmented DAC**, Technology Spectrum, Journal of JNTU, Volume 2 Issue 3 June 2008.
- Dr. C V Krishna Reddy, **Design and Simulation of Voltage to Current Converter**, Technology Spectrum, Journal of JNTU, Volume 1 Issue 2 July 2007.
- Dr. C V Krishna Reddy, **Design and Simulation of Differential Mode CMOS Voltage to Current Converter LE**, IJLE, Volume 7 Issue 3 September 2007.

Conferences / Seminars & Workshops attended:

- Ten Days Workshop on **Aspects of IC Design** at NIT Warangal, from 8th February to 17th February, 2016.

- Presented a paper on **A Novel Approach or Design and Implementation of Sequential Multiplier** in an international conference **ICCETMT-2015** organized by NNRG-Hyderabad on 12th December, 2015.
- Five days Faculty Develop Program on **Analog CMOS VLSI Design using Cadence Tools**, Organized by Entuple, Bangalore from 7th December to 11th December, 2015.
- Presented a paper on **Selecting Low power High speed Differential I/o for Continuous Time Sigma Delta ADC on VIRTEX-4 FPGA** in an international conference **ICCETMT-2015** organized by NNRG- Hyderabad on 12th December, 2015.
- Presented a paper on **H-spice modeling FPGA Low voltage Differential I/Os:LVDS,HSL-li and LVPECL for SD-ADC** in an international conference on Advanced Communications, VLSI and Signal Processing organized by GPCET on 11th April, 2015.
- Presented a paper on **Design and Implementation of Area optimized AES with S-Box Resource sharing based on FPGA** in an IETE Zonal seminar cum National symposium – Hyderabad, March 2014.
- Presented a paper on **High Speed differential amplifier based comparator for future FPGA/ASIC integrated sigma Delta ADC** in an IEEE international conference **ICARET** on 8th and 9th February 2013.
- Presented a paper on **Low 65dB SFDR, 500kS/s Continuous time All Digital Sigma Delta ADC for SONOR Applications** in an international conference **NAVCOM2012**, Hyderabad on 20th and 21st December, 2012.
- Presented a paper on **A Novel Architecture of LUT Design optimization for DSP Applications** in an international conference on **Electrical Electronics & Computer Science**, at Goa on 28th August, 2012.
- Presented a paper on **Design of an Efficient Reversible Logic Based Bidirectional Barrel shifter** in an international conference on **Electronics and Communication Engineering** at Bangalore on 20th May, 2012.
- Presented a paper on **Performance Analysis of First order Digital Sigma Delta ADC** in a 4th IEEE international conference **CICSN**, 2012.
- Presented a paper on **Low Power Design of Asynchronous protocol Converters for Two-phase Communications** in a national conference **RTANT-2015** organized by GNEC- Hyderabad on 29th July, 2011.
- Presented a paper on **A New Frame Work on Novel Area Efficient FPGA Architecture for FIR Filtering with Symmetric Signal Extension** in an International Conference **ACCIT**, Bangalore, December 2010.

- Five days International conference on **VLSI Design and Tutorials** at Hyderabad, conducted by VLSI Society of India, 2008.
- Presented a paper on **Design of low power CMOS transconductor** in an International Conference on simulation and modeling, CIT, Coimbatore, August 2007.
- Presented a paper on **Design of Low power high speed segmented DAC** in an International Conference on simulation and modeling, CIT, Coimbatore, August 2007.
- Presented a paper on **Design and simulation of CMOS Voltage to current converter** in an IETE Zonal seminar - Vishakhapatnam, February 2007.
- Five days International conference on **VLSI Design and Tutorials** at Hyderabad, conducted by VLSI Society of India, 2006.
- One week workshop on **DSP Tools and Practice** at IIT, Kharagpur, June 2006.
- Presented a paper on **A technique to reduce power consumption in Flash ADCs** in a national conference **NCAC** organized by PSGCT- Coimbatore, December 2005.
- One Week workshop on **VLSI Design**, Conducted by VLSI Society of India, Mysore, May 2005.
- Five days International conference on **VLSI Design and Tutorials** at Kolkata, conducted by VLSI Society of India, 2005.
- Two weeks STTP on **DSPAA** at NIT, Warangal, March, 2004.
- Presented a paper on **Performance Review of CMOS ADCs** in a national conference **NCVR** – Gwalior, February 2004.
- Three days National Workshop on **Microprocessors and Microcontrollers** at GNITs, Hyderabad, December 2003.
- Presented a paper on **Techniques to reduce power consumption in memories** in a national level Symposium organized by BRCE- Hyderabad, February 2003.
- Two weeks STTP on **VLSI design** at REC, Warangal, October, 2002.
- Three days National Workshop on **VLSI design** at ISSCT, Hyderabad, January 2001.
- Two weeks STTP on **High speed Networks** at REC, Warangal, October, 1999.

Guest lecturers delivered

- High level over view of VLSI Design at Vagdevi Engineering College, Warangal on 29th March, 2008.
- Analog IC Design, UGC refresher course on VLSI design and Embedded systems at Academic Staff College, JNTU, Hyderabad on 28th and 29th December, 2007.

- Layout design rules at UGC refresher course on VLSI design and Embedded systems at Academic Staff College, JNTU, Hyderabad, December, 2005.
- Layout design rules at UGC refresher course on VLSI design and Embedded systems at Academic Staff College, JNTU, Hyderabad on 23rd November, 2004.
- Micro Controllers Architecture & Programming at AICTE- ISTE -STTP on Micro Controllers and its Applications, KITS, Warangal from 7th to 9th June 2004.
- VHDL at VHDL work shop at KITS, Warangal on 17th & 18th February, 2003.
- Design rules at VLSI Design workshop at GNITS, Hyderabad on 15th December, 2004.

Patents filed:

- Title of the Invention: Washing Machine : 201741035618A,20-10-2017,36890
- Title of the Invention: Transportation Management System: 201741042490A,8-12-2017,47224

Memberships:

- S.M.I.E.E.E
- F.I.E.T.E
- M.I.S.T.E