NALLA NARASIMHA REDDY
Education Society's Group of Institutions - Integrated Campus
(Affiliated to JNTU Hyderabad, Approved by AICTE)
Academic Partnering with ORACLE ACADEMY

Dr C V Krishna Reddy, M.E, Ph.D.

Director, NNRG

Professional Memberships

Senior Member IEEE, Fellow IETE, Member ISTE

Educational Qualifications

- **Ph.D**. (ECE) JNTU, Hyderabad, June 2008
- **M.E.** (Applied Electronics) PSG College of Tech., Bharathiyar university ,Coimbatore, 1996 First Class (78%) GATE - 95.32
- **B.Tech.** (ECE) RVR & JC College of Engg.(N.U , Guntur) First Class 1989 (64%)
- **Intermediate** BSSB Jr College Tadikonda , Guntur Dt 1984 First class (76%)
- **SS** A P Residential School, Tadikonda , Guntur Dt 1982 First class (80%)

Administrative Assignments

- **Director,** Nalla Narasimha Reddy Education Society's Group of Institutions, Hyderabad, Sept 2011- till date
- **Dean**, School of Engineering, NNRESGI from July 2010-Aug 2011

- **Principal**,VSM Engg. College, Hyderabad May 2008- April 2010
- **Head** of ECE dept , KITS Warangal, Since April 2005 to May2008
- **Hony Secretary IETE Warangal** Sub Centre **,2003-2008**
- **Chairman IETE Warangal** Sub Centre, 2008-10
- **Member,** Board of Studies EIE, ECE, Kakatiya University , 2003-2007
- **Chairman** , Board of Studies ECE , Kakatiya University, Warangal-2007-2008
- Council member IETE (co-opted) 2012-2014

Professional Experience

- 25 years of Teaching Experience
- **Director**, Nalla Narasimha Reddy Education Society's Group of Institutions, Hyderabad, Sept 2011- till date
- **Dean**, School of Engineering, NNRESGI, July 2010 to April2011
- **Principal,** VSM Engg. College, Hyderabad May'08 to April 2010
- **Associate professor,** KITS , Warangal **,** Feb 1998 to May 2008
- **Sr Lecturer,** Vellore Institute of Technology, Vellore, May 97 to Feb 98
- **Lecturer**, BLDEA's College of Engg. Bijapur June 90 to May 97

Short Term programs/Workshops Attended

- 2 Week STTP on High speed Networks at REC Warangal(Oct 99)
- 3 day Workshop on VLSI design at ISSCT Hyderabad(Jan 01)
- 2Week STTP on VLSI design at REC, Warangal(Oct 02)
- 3 Day workshop on Microprocessors and Microcontrollers, GNITS, Hyderabad (Dec2003)
- 2Week STTP on DSPAA at NIT, Warangal (Mar 2004)
- 5 Days International conference on VLSI Design-2005 and Tutorials at Kolkata , conducted by VLSI Society of India
- One Week work shop on VLSI Design ,Conducted by VLSI Society of India ,Mysore, May 2005
- One week work shop on DSP Tools and Practice ,IIT, Kharagpur, June 2006
- 5 Days International conference on VLSI Design-2006 and Tutorials at Hyderabad , conducted by VLSI Society of India
- 5Days International conference on VLSI Design-2008 and Tutorials at Hyderabad , conducted by VLSI Society of India
- 5day FDP on Analog CMOS VLSI Design using Cadence Tools Organized by Entuple, Bangalore from Dec7-11.2015
- 10Days Work shop on "Aspects of IC Design" NIT Warangal, 8th Feb-17th Feb 2016

Guest lecturers delivered

- High level over view of VLSI Design at Vagdevi Engg. Colllege, Warangal, 29th March,2008
- Analog IC Design, UGC refresher course on VLSI design and Embedded systems at Academic Staff College ,JNTU ,Hyderabad 28,29Dec 2007
- Layout design rules at UGC refresher course on VLSI design and Embedded systems at Academic Staff College ,JNTU ,Hyderabad Dec 2005
- Layout design rules at UGC refresher course on VLSI design and Embedded systems at Academic Staff College ,JNTU ,Hyderabad.23rd Nov' 2004
- Micro Controllers Architecture &Programming at AICTE- ISTE -STTP on Mcro Controllers and its Applications ,KITS, Warangal 7th,8th,9th June 2004
- VHDL at VHDL work shop at KITS ,Warangal 17th & 18th Feb '2003
- Design rules at VLSI Design workshop at GNITS, Hyderabad on 15thDec'04

Publications-Journals

1. Design of STT-RAM cell in 45nm hybrid CMOS/MTJ Int. Jou. Of Science and Engg Applications ISSN-2319-7560 (Vol.3 Issue 3 May-June2014 Pp 49-52
2. An Alternative Logic Approach to Implement Energy Efficient 90-Nm CMOS full adders Int Jou of Scientific research ISSN 2277-8179Vol 2 Issue 10 Oct Pp 70-73
3. Design of an Efficient Reversible Logic Based Bidirectional Barrel shifter International Journal of Electronics Signals and systems (IJESS) ISSN: 2231-5969 Vol-2, 2,3,4,, 2012, p.p.No. 48-53.
4. Optimum Decimation and Filtering for reconfigurable Sigma Delta ADC Far East Journal of Electronics and Communications ISSN 0973-7006Volume 11, Issue2Dec 2013 Pages 101 - 111
5. An Alternative Logic Approach to Implement Energy Efficient 90-nM CMOS Full Adders International Journal of Scientific Research(IJSR)ISSN 2277-8179Vol. 2Oct 2013Pp 1-3
6. An Improved Optimization Techniques for Parallel Prefix Adder using FPGA .Techniques for Parallel Prefix Adder using FPGA International Journal of Modern Engineering Research (IJMER) www.ijmer.com Vol. 3, Issue. 5, Sep - Oct. 2013 pp-3107-3115 ISSN: 2249-6645 International Journal of Modern Engineering Research (IJMER) ISSN: 2249-6645 Vol.3 issue 5 2013 pp-3107-3115
7. A Novel Architecture of LUT Design Optimization for DSP Applications International Journal of Advanced Electrical and Electronics Engineering, ISSN (Print): 2278-8948Vol.-1, Issue-22012 p.p No 1-6
8. Analysis on Digital Implementation of Sigma-Delta ADC with passive analog components International Journal of Computing and Digital systems: ISSN 2210-142XVol. 2 2013 Pp 71-77
9. Design and Simulation of Voltage to Current Converter, "Technology Spectrum, Journal of JNTU, Vol. 1, No.2 , July 2007
10. Design of Low power high speed segmented DAC Technology Spectrum, Journal of JNTU, Vol..2,

No.3 June 2008

11. Design and Simulation of Differential Mode CMOS Voltage to Current Converter LE Journal of Laboratory experiments Vol. 7,NO.3Sept2007 pp 220-224
12. Power Optimization in Flash ADCs "Far East International Journal of EC ISSN 0973 – 7006,Vol.No.3,Dec2008
13. Design and Implementation of Reversible Logic Based Bidirectional Barrel Shifter 978-1-4673-2396- 3/12 IEEE-ICSE2012 Proc., 2012, Kuala Lumpur, Malaysia.2012 p.p. 490-494

Conferences

1. A Novel Approach or Design and Implementation of Sequential Multiplier, International conference on Challenges and Emerging trends in Management&Technology-2015, NNRES, Hyderabad on 12th Dec, 2015.
2. Selecting Low power High speed Differential I/o for Continuous Time Sigma Delta ADC on VIRTEX-4 FPGA, International conference on Challenges and Emerging trends in Management&Technology-2015, NNRES, Hyderabad on 12th Dec, 2015.
3. H-spice modeling FPGA Low voltage Differential I/Os:LVDS,HSL-Ii and LVPECL for SD-ADC, International conference on Advanced Communications, VLSI and Signal Processing, 11th April2015 , G Pullaiah college of Engineering& Technology.
4. A Novel Architecture of LUT Design optimization for DSP Applications." International conference on Electrical Electronics & Computer Science, ISBN: 987-9381361-17-7,28th August, 2012, GOA, p.p. No. 17-22
5. Design of An Efficient Reversible Logic Based Bidirectional Barrel shifter ", International Conference in Electronics and Communication Engineering, ISBN: 978-93-81693-29-2, 20th May 2012, Bangalore p.p.No. 108-114.
6. Low Power Design of Asynchronous protocol Converters for Two-phase Communications" day National Conference on Recent Trends and Advances in Nano Technology, Guru Nanak Engineering College, Hyderabad.. 29th July, 2011
7. 65dB SFDR, 500kS/s Continuous time All Digital Sigma Delta ADC for SONOR Applications Peer jubilee international conference on Navigation and Communication NAVCOM2012 Hyderabad Dec 20-21. 2012328-331
8. High Speed differential amplifier based comparator for future FPGA/ASIC integrated sigma Delta ADC IEEE ICARETFeb8-9th 2013,365-369
9. Performance Analysis of First order Digital Sigma Delta ADC 4th International conference on computational Intelligence, Communication systems and Netwotks978-0-7695-821CICSyN0/12@2012 IEEE 2012 435-440
10. Techniques to reduce power consumption in memories National level Symposium , Bhoj Reddy College of Engg Hyderabad, Feb 2003
11. Performance Review of CMOS ADCs, National Conference, NCVR Gwalior (Feb'04)
12. . A technique to reduce power consumption in Flash ADCs 4.National conference NCAC ,PSG College of Tech Coimbatore Dec 2005

13. Design and simulation of CMOS Voltage to current converter IETE Zonal seminar, Vishakapatnam Feb 2007
14. Design of low power CMOS transconductor6.,International Conference on simulation and modeling ,CIT, Coimbatore, Aug - 2007
15 . Design of Low power high speed segmented DAC,7International Conference on simulation and modeling ,CIT, Coimbatore, Aug 2007
16. A New Frame Work on Novel Area Efficient FPGA Architecture for FIR Filtering with Symmetric Signal Extension, International conference on Advances in computing, communication and information Technologies ACCIT-2010, Dec 2010 ,Bangalore
17. Design and Implementation of Area optimized AES with S-Box Resource sharing based on FPGA IETE Zonal seminar cum National symposium, Hyderabad28-30March 2014

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